Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	246-97-004
Total Pages	20
First Named Inventor or Application Identifier	RONALD F. WELCH, JR. ET AL.
Express Mail Label No.	EF223617397US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form (IN DUPLICATE) *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 8] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets 7] INFORMAL
4. Oath or Declaration [Total Pages 2] UNEXECUTED
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* *[Note Box 5 below]*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney *(when there is an assignee)*
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [ ] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label *(Insert Customer No. or Attach bar code label here)* or [X] Correspondence address below

NAME	Verne E. Kreger, Jr.				
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FEE TRANSMITTAL

Note: Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 790.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	RONALD F. WELCH ET AL. JR
Group Art Unit	
Examiner Name	
Attorney Docket Number	246-97-004

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 01-1113

Deposit Account Name:

[ ] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [ ] Payment Enclosed: [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	
				SUBTOTAL (1)	($)

2. CLAIMS

			Extra		Fee from below		Fee Paid
Total Claims	8	-20 =	0	X	22	=	0
Independent Claims	3	- 3 =	0	X	82	=	0
Multiple Dependent Claims				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	
				Other fee (specify)	
				Other fee (specify)	
				* Reduced by Basic Filing Fee Paid SUBTOTAL (3)	($)

SUBMITTED BY			
Typed or Printed Name	Verne E. Kreger, Jr.	Complete (if applicable) Reg. Number	35,231
Signature	Verne E. Kreger Jr.	Date 8/17/98	Deposit Account User ID

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EF223617397US

Attorney Docket No. 246-97-004

UNITED STATES PATENT APPLICATION FOR:

METHOD FOR FLUORESCENT LAMP DIMMING CONTROL

Background of the Invention

A means of varying fluorescent light intensity is required in certain applications, such as in avionics, especially at low ambient light levels. Currently, high-frequency switching supplies are used, although at low brightness levels such supplies suffer from non-uniform brightness across the display and flickering caused by arc instability. Superior results have been achieved by utilizing separate supplies for high and low brightness ranges, and switching between them to obtain the desired level of brightness.

Brief Description of Drawings

Figure 1 is a schematic diagram of a power supply for a fluorescent lamp;

Figure 2 is a schematic diagram of a voltage-based low brightness supply;

Figure 3 is a waveform diagram of the output of the voltage source in the circuit of Figure 2;

Figure 4 is a schematic diagram of a current-based low brightness supply;

Figure 5 is a schematic diagram of a configuration of the voltage-based low brightness supply of Figure 2;

Figure 6 is a waveform diagram of drive signals for the low brightness supply of Figure 5;

Figure 7 is a schematic diagram of an implementation of the voltage-based low brightness supply of Figure 5;

Figure 8 is a schematic diagram of a configuration of the current-based low brightness supply of Figure 4; and

Figure 9 is a schematic diagram of an implementation of the current-based low brightness supply of Figure 8.

Description of the Invention

A power supply for a fluorescent lamp is shown in the schematic diagram of Figure 1. A fluorescent lamp 10 is powered by two power supplies: a high brightness supply 30 and a low brightness supply alternately connected through a relay K1. The high brightness supply 30 generates an output voltage that will ignite the gas in the lamp 10 so that it produces its normal level of brightness. If a lower level of brightness is desired, the relay K1 switches, connecting the low brightness supply 40. The voltage level of the low brightness supply 40 is below the ignition voltage and therefore the gas in the lamp 10 will not ignite but rather operates in the glow mode or glow discharge mode. Thus, the lamp 10 is switched back and forth between the two supplies as necessary to achieve the brightness desired.

A low brightness power supply and a lamp are shown in Figure 2. There, an ideal voltage source v having a source resistance R_S drives the lamp 10. A suitable waveform for the voltage source output is shown in Figure 3. Here, the waveform is a bipolar pulse-width modulated square-wave. In the example shown in Figure 3, the pulses begin at full width per half cycle (i.e., 100% duty cycle), but are only half of that width after the first three cycles, signifying a change in brightness. By varying the pulse width, the RMS voltage applied to the lamp 10 and, therefore, the observed

intensity of the lamp 10 similarly varies. Other types of waveforms could be employed (e.g., triangular, sawtooth, sinusoidal). Further, the pulse widths could be varied at the leading or trailing edge.

The constant-current equivalent of Figure 2 is illustrated in Figure 4. There, a constant current source I drives the lamp 10. The same waveform used with Figure 2 can be employed here, the vertical axis being current i instead of voltage v.

A configuration of the voltage-based low brightness supply of Figure 2 is shown in Figure 5. In this circuit, a voltage source V_{DC} is alternately connected to one side or the other of the lamp 10 by switches S_1 and S_2 controlled by voltage generators v_1 and v_2, respectively. These generators produce complementary (180° out of phase) pulse-width modulated square wave signals v_1 and v_2, with duty cycles varying from 0 to 100% (100% being the full half-cycle pulse width) in a frequency range of 60-400 hz. Satisfactory results have been obtained at approximately 100 hz. Typically, the generators are tied to a synchronous clock. Examples of the drive signals are shown in Figure 6. Of course, other waveforms and frequency ranges could be employed.

A more specific implementation of the low brightness supply of Figure 5 is illustrated in Figure 7. The connections to the high brightness supply are omitted for clarity but it should be understood that such a supply could be used with this circuit.

Each side of the lamp 10 is connected to the junction of a load resistor R_1 or R_2 and a switching transistor Q_1 or Q_2. The resistors are chosen to insure that the lamp 10 operates in the glow mode for a given supply voltage. Assuming a supply voltage V_{DC} of 400 volts, a desired lamp voltage of 200 volts, and a lamp resistance of 100K, the load resistors of 100K can be employed. Other voltages and values can be chosen to suit the components and desired design criteria.

When the switching transistors are off, both terminals of the lamp 10 are sitting at the supply voltage V_{DC}. The gates of the switching transistors Q_1 and Q_2 are driven by signals v_1 and v_2, respectively, the duty cycles of which are varied to achieve the desired brightness level.

The circuit in Figure 7 uses a voltage divider of a load resistor R_1 or R_2 and the internal resistance of the lamp 10 to provide a set voltage at the lamp 10 and in turn a predetermined current through the lamp 10. The diode D prevents the source voltage of either Q_1 or Q_2 from going negative and prematurely turning the other transistor on while the resistor R_C limits the current drawn by the parasitic capacitance of the switching transistors.

A configuration for the current-based low brightness supply of Figure 4 is shown in Figure 8. The lamp 10 is driven by a constant current source I in alternating opposite directions by switches S_1 and S_2 controlled by voltage generators v_1 and v_2, respectively. An implementation of the circuit of Figure 8 is shown in Figure 9. The lamp 10 is flanked on each side by a buffer (Q_1 and R_1, or Q_2 and R_2) and a source-follower (Q_3 and R_3, or Q_4 and R_4). The buffers are driven by the voltage generators v_1 and v_2. The current through the lamp 10 is determined by the gate voltage of either Q_1 or Q_2, less the gate-to-source drop, divided by the value of the load resistor R_L. Assuming a gate input voltage of 12 volts and a gate-to-source drop of 3 volts, and value of 2.4 K for the load resistor R_L, the current will then be 3.75 ma.

The diodes D_1 and D_2 protect the gate-source junctions of Q_3 and Q_4 by preventing the voltage across those junctions from reaching an excessive level whenever the transistors are switched.

Similar to the diode in Figure 7, diode D_3 prevents Q_1 and Q_2 from turning on as a result of the source voltage going to less than zero when the drive is zero. The

series combination of C_1 and R_5 has a short time constant and provides a charging circuit for the parasitic capacitances of the transistors Q_1 and Q_2. The arrangement in Figure 9 dissipates less power than the voltage-based circuits because the circuit uses current control to vary the brightness of the lamp 10, instead of large voltage drops across load resistors.

In operation, the circuit of Figure 1 can provide variable light output over a broad range. At the high end of brightness, the high brightness supply 30 can be configured to provide sufficient energy to the lamp 10 to produce a variable light intensity from a maximum value, determined by the characteristics of the lamp 10 and voltage applied to the lamp 10, down to some minimum value. The lamp in this circumstance operates mostly in the arc discharge mode or region, and perhaps partially in the glow discharge region. After a transition, e.g., by switching the relay K1, the low brightness supply 40 provides energy to the lamp 10, maintaining the voltage on the lamp 10 to a level that keeps the operation of the lamp 10 in the glow discharge mode or region. When powered by the low brightness supply 40, the lamp's output is more uniform at very low luminance levels.

If desired, the components, voltages, duty cycles, and other parameters can be chosen to provide an overlap between the high and low brightness ranges. A slight overlap between the high and low ranges will avoid any discontinuity in brightness.

What is claimed is:

1. A system, comprising:

a fluorescent lamp;

first means for providing electrical energy to the lamp to produce a first range of brightness; and

second means for providing electrical energy to the lamp to produce a second range of brightness, where the lamp operates in the glow discharge mode.

2. A system as set forth in claim 1, further comprising means for switching between the first and second means for providing electrical energy.

3. A system as set forth in claim 1, where the second means for providing electrical energy comprises a source of pulse-width modulated bipolar voltage or current of a level sufficient to maintain the operation of the lamp in the glow discharge mode.

4. A system as set forth in claim 3 where the bipolar voltage or current is a low frequency square wave signal.

5. A system as set forth in claim 1, where the first and second ranges of brightness overlap.

6. A low brightness supply for a fluorescent lamp, comprising a source of pulse-width modulated bipolar voltage or current of a level sufficient to maintain the operation of the lamp in the glow discharge mode.

7. A low brightness supply as set forth in claim 6 where the bipolar voltage or current is a low frequency square wave signal.

8. A power supply system for a fluorescent lamp, comprising:

a first power supply for providing electrical energy to the lamp to produce a first range of brightness, where the first power supply comprises a source of high-frequency voltage or current;

a second power supply for providing electrical energy to the lamp to produce a second range of brightness, where the second means for providing electrical energy comprises a source of low-frequency, pulse-width modulated bipolar voltage or current of a level sufficient to maintain the operation of the lamp in the glow discharge mode; and

a switch for switching between the first and second power supplies.

Abstract

A broad range of brightness in a fluorescent lamp may be achieved by applying low-frequency, pulse-width modulated voltage or current to the lamp for a low level of brightness, or high-frequency voltage or current for a high level of brightness. Switching is provided to select between the two signals.

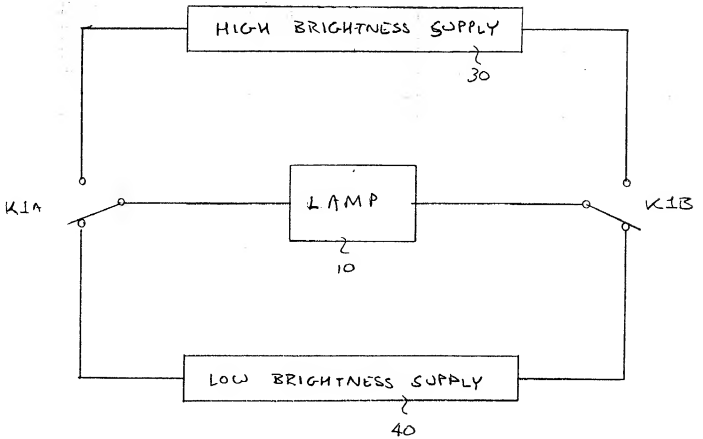
HIGH BRIGHTNESS SUPPLY
30
LAMP
10
K1A
K1B
LOW BRIGHTNESS SUPPLY
40

FIG. 1

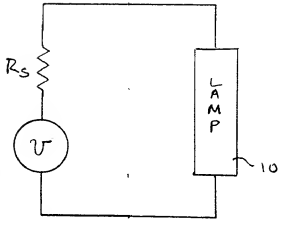

FIG. 2

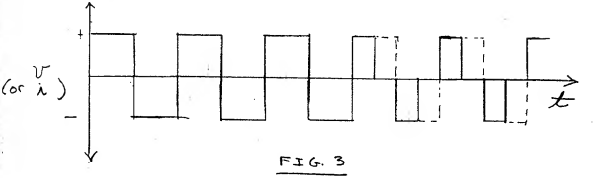

FIG. 3

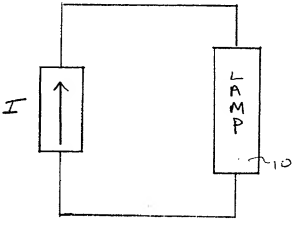

FIG. 4

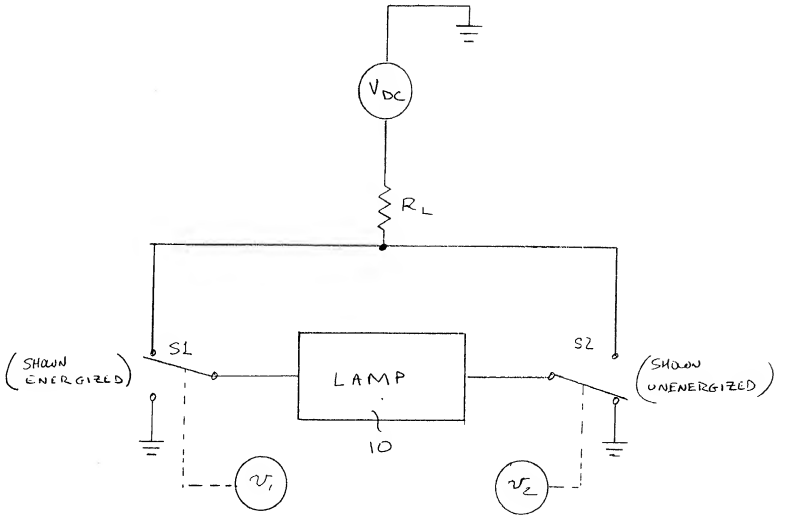

FIG. 5

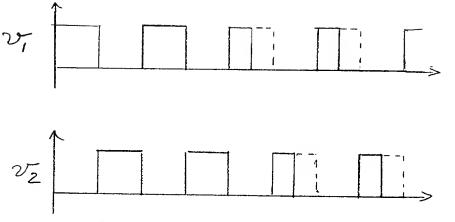

FIG. 6

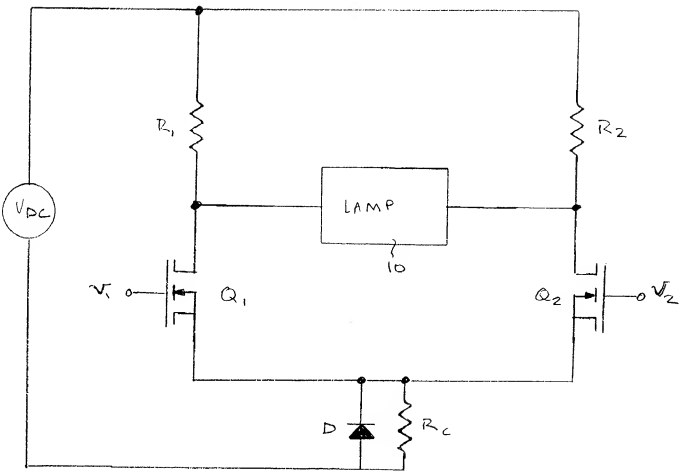

FIG 7

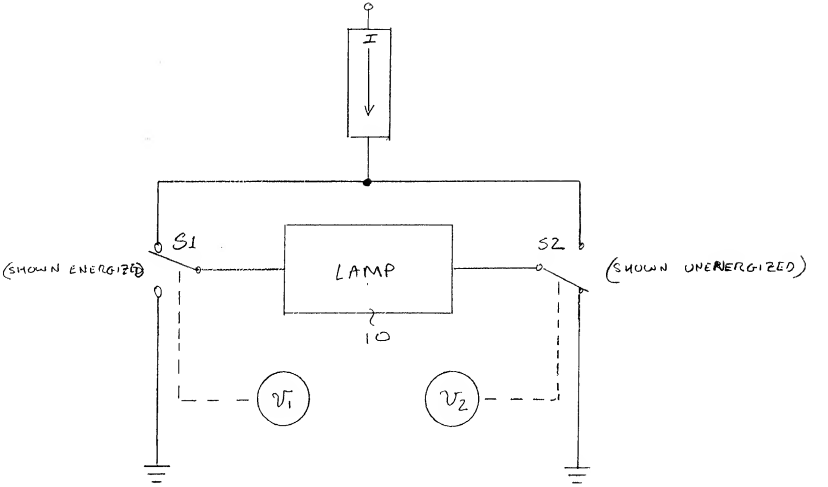

FIG. 8

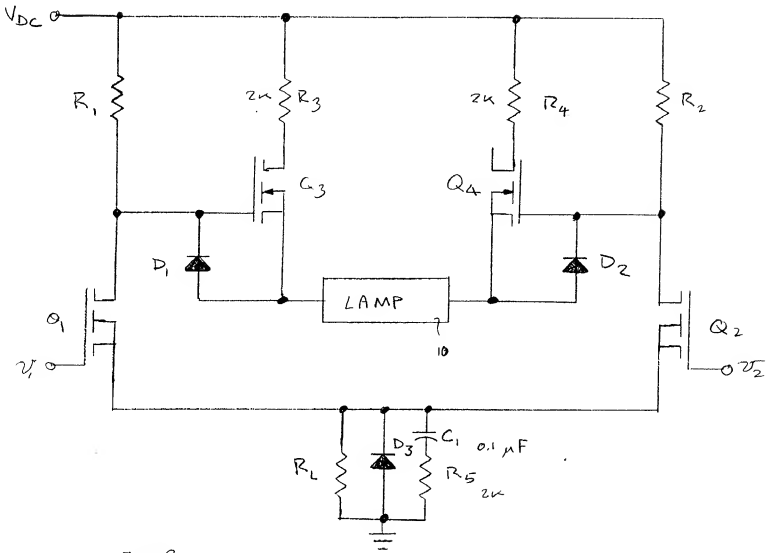
V_{DC}
R_1
2K
R_3
2K
R_4
R_2
C_3
Q_4
D_1
D_2
LAMP
10
Q_1
Q_2
V_1
V_2
D_3
C_1 0.1 μF
R_L
R_5 2K

FIG 9

Attorney's Docket No.: 246-97-004

DECLARATION FOR PATENT APPLICATION
SOLE OR JOINT

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention titled:

Method For Fluorescent Lamp Dimming Control

I HEREBY STATE THAT I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS

I ACKNOWLEDGE THE DUTY TO DISCLOSE INFORMATION WHICH IS MATERIAL TO THE EXAMINATION OF THIS APPLICATION IN ACCORDANCE WITH TITLE 37, CODE OF FEDERAL REGULATIONS, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States applications listed below and, INSOFAR AS THE SUBJECT MATTER OF EACH OF THE CLAIMS OF THIS APPLICATION IS NOT DISCLOSED IN THE PRIOR UNITED STATES APPLICATION IN THE MANNER PROVIDED BY THE FIRST PARAGRAPH OF TITLE 35, UNITED STATES CODE, §112, I ACKNOWLEDGE THE DUTY TO DISCLOSE MATERIAL INFOMATION AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, §1.56(a) WHICH OCCURRED BETWEEN THE FILING DATE OF THE PRIOR APPLICATION AND THE NATIONAL OR PCT INTERNATIONAL FILING DATE OF THIS APPLICATION:

**

(Application Serial Number)	(Filing Date)	(STATUS: Patented, Pending, Abandoned)
(Application Serial Number)	(Filing Date)	(STATUS: Patented, Pending, Abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected herewith (List name and registration number).

(LIST SENIOR PATENT COUNSEL AND ATTORNEY HANDLING CASE WITH PATENT OFFICE REGISTRATION NUMBERS.)

Verne E. Kreger, Jr.	John Donofrio	
Name	Name	Name
35,231	32,339	
Registration Number	Registration Number	Registration Number

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Teterboro, New Jersey 07608

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Oak Ridge, New Jersey 07438

FULL NAME OF SECOND JOINT INVENTOR William R. Tombs
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CITIZENSHIP USA
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FULL NAME OF THIRD JOINT INVENTOR Muthu Murugan
INVENTOR'S SIGNATURE _____ Date _____
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POST OFFICE ADDRESS 39 Peach Stone Road
Howell, New Jersey 07731

FULL NAME OF FOURTH JOINT INVENTOR Robert Saccomanno
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Montville, New Jersey 07045

FULL NAME OF FIFTH JOINT INVENTOR
INVENTOR'S SIGNATURE _____ Date _____
RESIDENCE
CITIZENSHIP
POST OFFICE ADDRESS